## REMARKS/ARGUMENTS

Applicants file this continuation application and Preliminary Amendment to prosecute various claims from the parent case Serial No. 09/878,985. In the parent case 09/878,985, the Examiner: (1) objected to claims 2 and 5; (2) rejected claims 1, 2. 4-6 and 16-18 as anticipated by Computer Architecture: A Cumulative Approach by Patterson and Hennessy (herein referred to as "Patterson"); (3) rejected claims 19-21 as anticipated by Safranek (U.S. Pat. No. 6,493,809); (4) rejected claims 11 and 15 as obvious over the combination of Patterson and Safranek; and (5) rejected claims 12-14 as obvious over Patterson in view of Laudon (U.S. Pat. No. 5,634,110). In an Office Action dated March 13, 2003, the Examiner indicated claims 3 and 7-10 were allowable, but by telephone on August 21, 2003, subsequently withdrew the allowance of claims 3 and 7 and continued to allow claims 8-10.

In this continuation, Applicants have resubmitted claims 1-7 and 11-21 as originally submitted in the parent case with claims 1, 2, and 5 being further amended. Having been allowed in the parent case, claims 8-10 are canceled.

The objections to claims 2 and 5 have been addressed by amendment as shown above. These amendments do not narrow the scope of the claims.

Regarding the art rejections, claim 1 requires a protocol engine that implements a cache coherence protocol. The claimed protocol engine sends an initial invalidation request to no more than a first predefined number of nodes associated with bits that are set in an identification field of a directory entry. Applicants amend claim 1 to require that "the first predefined number of nodes being greater than one, but less than the number of nodes associated with set bits in the identification field." As such, the protocol engine sends at least two invalidation requests, but fewer invalidation requests than the number of nodes associated with the set bits in the identification field. A bit that is set in the identification field signifies that the memory line associated with that identification field is cached in at least one associated node.

The Examiner rejected claim 1 as anticipated by Patterson. Patterson generally discloses a bit vector in which each bit indicates whether a corresponding processor has a copy of a block of a particular data. See

Patterson, page 680. However, Patterson discloses sending all processors identified in the bit vector as having a copy of the block invalidation messages. Patterson page 685 ("All processors in the set Sharers are sent invalidate messages...."). Thus, Patterson does not teach or suggest sending an initial invalidation request to more than one, but less than the number of nodes associated with set bits in an identification field.

Although the Examiner did not use Safranek or Laudon to reject claim 1, Applicants contend claim 1 is patentable over Safranek and Laudon. Safranek discloses several embodiments. In Figures 1A-1C and associated text at col. 9 lines 14-64, Safranek teaches a "head" node sending invalidation requests to all nodes needing to be invalidated. In Figures 7A-7C and associated text at col. 9 line 64-col. 10, line 36, Safranek also teaches the head node sending invalidation requests to all nodes needing to be invalidated, albeit with a degree of concurrency. In Figures 9A-9C and associated text at col. 11 line 64-col. 12, line 11, Safranek also teaches forwarding an invalidation request from one node to another node. In the embodiments of Figures 1A-1C and 7A-7C, the head node sends requests to all nodes, while in the embodiment of Figure 9, the head node only sends one invalidation request. As amended, claim 1 requires sending an initial invalidation request to more than one other node, but less than the number of nodes associated with set bits that indicate the nodes that have cached the associated memory line. Safranek, therefore, does not teach or suggest this feature of claim 1.

Laudon teaches fine and coarse bit vectors, but does not teach or suggest sending initial invalidation requests to a first predefined number of nodes "being greater than one, but less than the number of nodes associated with set bits in the identification field." Laudon, therefore, also does not teach or suggest all of the limitations of claim 1. Moreover, none of the cited art teaches or suggests the above-discussed feature of claim 1. For at least this reason, claim 1 is allowable. Claims 2-7 and 11-18 depend on or from claim 1 and thus are patentable for at least the same reason as claim 1.

Independent claim 19 requires, among other limitations, input logic that receives a first invalidation request identifying a memory line and including a

pattern of bits for identifying a subset of the nodes that potentially store cached copies of the memory line. Claim 19 also requires processing circuitry that sends a second invalidation request corresponding to the first invalidation request to a next node if the bits in the first invalidation request in fact identify the next node.

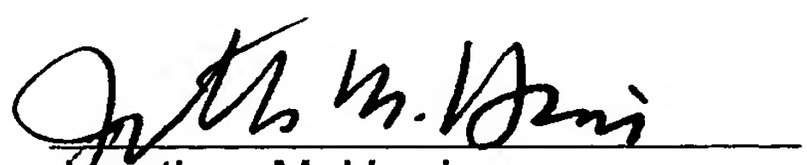
The Examiner rejected claim 19 as anticipated by Safranek. Safranek, however, does not appear to teach or even suggest including bits in the invalidation requests that identify nodes that potentially store cached memory lines. By contrast, Safranek discloses the use of a "sharing list" that identifies the nodes that share a line of memory. Safranek does not disclose that the sharing list is transmitted as part of the invalidation requests. None of the other cited art satisfy the deficiency of Safranek. At least for this reason, claim 19 is allowable.

Claim 20 also requires input logic that receives a first invalidation request identifying a memory line and including a pattern of bits for identifying a subset of the nodes that potentially store cached copies of the memory line. Further, claim 20 comprises processing circuitry for determining a next node identified in the bits from the invalidation request. As explained above, Safranek does not appear to teach or suggest including bits in the invalidation requests that identify nodes that potentially store cached memory lines. The other art appears deficient as well.

Applicants respectfully request reconsideration and allowance of the pending claims. If any fees or time extensions are inadvertently omitted or if any fees have been overpaid, please appropriately charge or credit those fees to Hewlett-Packard Company Deposit Account Number 08-2025 and enter any time extension(s) necessary to prevent this case from being abandoned.

Applicants respectfully request that a timely Notice of Allowance be issued in this case.

Respectfully submitted,



Jonathan M. Harris
PTO Reg. No. 44,144
CONLEY ROSE, P.C.
(713) 238-8000 (Phone)
(713) 238-8008 (Fax)
ATTORNEY FOR APPLICANTS

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
Legal Dept., M/S 35
P.O. Box 272400
Fort Collins, CO 80527-2400